Cornelius
Oregon's Family Town

Cornelius
All-America City
NATIONAL CIVIC LEAGUE
2019

February 22, 2023

Hon. Senator Janeen Sollman, Co-Chair
Hon. Representative Janelle Bynum, Co-Chair
Hon. Joint Committee Members
Joint Committee on Semiconductors
900 Court Street NE, Room 453
Salem, OR 97301

Re: Supplemental Cornelius Testimony: Semiconductor Manufacturing Supply Chain in Cornelius

Dear Senator Sollman, Representative Bynum and Joint Committee Members,

Thank you for considering this third testimony from the City of Cornelius. It speaks to how a legislative 430-acre industrial UGB expansion next to Cornelius will provide semiconductor supply chain sites (and companies) just minutes away from potential future large semiconductor manufacturing fab sites adjacent to both North Plains and Hillsboro recommended by the *Semiconductor Manufacturing Competitiveness Task Force* ("Task Force" herein.)

Based on Committee testimony from Messer, Sheehy, Leavitt, Gupta and others, we explain how and why adding our expansion land area for supply chain users to Oregon's CHIPS Act Funding Proposal ('Proposal") application is essential for the application to be complete, holistic, competitive and persuasive to the US Commerce Department. Our testimony focuses on the "land need" element of the four (4) semiconductor manufacturing inducement pillars (land need, financial and other incentives, workforce equity and cash input) being examined by the Committee.

From that land-need perspective, the discussion below addresses: (1) CHIPS Act Proposal Completeness, (2) Semiconductor Supply Chain, (3) Supply Chain Site Readiness, (4) Workforce Equity and (5) Oregon's Land Use System Application. Testimony received by the Committee supports the discussion.

I. Oregon Chips Act Proposal Completeness

Committee discussions described two Proposal "completeness" facets: (1) a semiconductor manufacturing industry ecosystem land need and benefits perspective described by Dick Sheehy and semiconductor industry representatives, and (2) a Legislative "bold roadmap" CHIPS Act Proposal approach advised by Vice Chair Senator Knopp. Each is summarized below. Each would be achieved by enabling supply chain companies to locate on the 430-acre Cornelius UGB expansion area.

a. Industry need/benefits perspective:

At the February 1 Joint Committee Meeting, speaking to the land-need perspective, Mr. Sheehy explained that, traditionally, large semiconductor fabs will require their suppliers to also locate and build nearby within a fab's "network location." Thus, there will be "suppliers' opportunities" if a large fab locates and develops. He explained at the January 30 Meeting that while large fabs drive a big supply chain, most jobs created come from the supply chain companies. He further explained that sites for semiconductor manufacturing suppliers do not exist in the proposed sites in many of the other states competing for CHIPS Act funds. Therefore, including such sites in Oregon's Proposal will be an "Act advantage." At the February 1 meeting, Group Mackenzie Consulting reported that Oregon has only one (1) site, in Woodburn, that can meet Mr. Sheehy's criteria regarding sites needed for key material suppliers.

b. A "Bold Roadmap" Approach

At the February 8 Joint Committee meeting, Vice Chair Knopp opined that a strong, successful Oregon CHIPS Act proposal means not just getting one or two manufacturing fabs; it must include an entire set of semiconductor ecosystem companies (big and small), manufacturers and suppliers, that produce a lasting tech-economy base capable of providing good jobs for generations. At the February 13 meeting, U.S. Congresswoman Bonamici explained that the CHIPS Act also focuses on "back-end packaging facilities" that surely include the array of companies referenced by Senator Knopp.

Senator Knopp urged the Legislature to "be bold" and "think big" and that Committee failure on this matter is not an option in part because of semiconductor manufacturing national security concerns. He urged the Legislature to provide a "roadmap" for companies interested in Oregon sites to prepare their part of an Oregon public-private winning CHIPS Act application. (We understand part of his "roadmap" to mean superior-performing Oregon commitments in addressing and delivering on the 4-part application "pillars" cited above – which includes delivering proposed manufacturing and supply chain land even if this is not necessarily done "like it's always done" relying on Oregon Land Use System requirements.)

Moreover, although stated differently, that bold approach was also advised by Keith Leavitt, Task Force advisor at the January 30 Meeting. He advised that looking only to provide two 500-acre sites misses the point of what the CHIPS Act and the Task Force is recommending: a "holistic approach" in Oregon's semiconductor proposal. This advice permeates Senator Knopp's remarks. It was also given by Mr. Gupta (Cascade Manufacturing) as cited below.

II. Semiconductor Supply Chain Components

At the January 18 Joint Committee meeting, Duncan Wyse explained that the Task Force's Vision includes expansion of all existing device manufacturing and parts suppliers; developing a cluster of leading-edge fab-less chip designers (such as Lattice Semiconductor, Ampere); encouraging more R&D product development (i.e., Analog, Lam Research) and ensuring a strategic, responsive supply of sites that meet semiconductor manufacturing industry needs. All these types of semiconductor ecosystem companies are integral and essential to semiconductor chip manufacturing supply-chain contributors.

The 430-acre Cornelius UGB expansion area's close proximity and direct access to the two identified Washington County 500-acre sites present considerable semiconductor chip manufacturing, production, problem-solving, machine repair, and component-parts delivery that cannot be matched by other potential supply chain locations presented to the Committee. This proximity makes this area the best option for ensuring a cost-efficient and rapid production "symbiotic" working relationship between semiconductor chip manufacturing at large fab sites and various "semiconductor assembly" supply chain

companies identified below and described to the Committee by Sanjay Gupta (Cascade Manufacturing) at its February 1 meeting.

The critical importance of including land for supply chain companies in Oregon's CHIPS Act Proposal is their "semiconductor assembly" role in a six-steps chip manufacturing process: deposition, photoresist, lithography, etching, ion implanting and packaging (each step is described in Attachment 1) At the January 18 and February 1 Joint Committee meetings Mr. Gupta explained that Oregon needs to look at its CHIPS Act Proposal effort "holistically" and help expand or attract existing technology companies that make the products and services that enable fabs to manufacture semiconductor chips. That concept was affirmed by Dick Sheehy at the January 30 meeting. He explained that fabs drive a big supply chain and thus land should be added to Oregon's Proposal for supply chain companies.

III. Supply Chain Site Readiness:

The attached 430-acres UGB expansion area map depicts where semiconductor supply chain companies would be accommodated within three (3) potential business parks containing approximately 320, 175 and 143 acres respectively. All three sites have substantially flat profiles and they abut Susbauer Road, a designated truck-route which connects the area to the two 500-acre sites in Hillsboro and North Plains, with travel distance of roughly 10-15 minutes. All three sites would connect to existing water and sewer mains located along the City Limit directly to their south.

While the cost of providing sewer, water and power infrastructure needed to serve the three potential business parks would be considerable, on-site costs are private development costs to be borne by supply chain companies that locate within the business parks. Off-site costs are public-sector responsibilities and would be covered by a combination of negotiated City-developer/company rezoning conditions and development agreements covering infrastructure costs outside of those covered by the City. Additionally, Oregon and Cornelius would likely be able to capture "back-end packaging facilities" CHIPS Act funds that U.S. Congresswoman Bonamici referenced as supporting semiconductor supply chain site developments.

Finally, the 430-acre site has the same "undeveloped land" characteristic as do the two 500-acre sites and, thus, shares with those sites the same infrastructure limitations and opportunities should all three areas be added to the UGB by the Legislature.

IV. Workforce Equity

Section 9902 of the CHIPS Act requires "commitments" that will "*expand employment opportunity for economically disadvantaged individuals"* and *"provide workforce training . . . to be eligible for funding."* At the February 1 meeting Clark Williams noted the Act's preference regarding serving low-income communities and disadvantaged groups. In essence Section 9902 pertains directly to a clear Committee objective to pursue "shared prosperity" and achieve "workforce – and thus family – equity" in the job-creating impacts of a successful Oregon CHIPS Act Proposal.

At the January 18 meeting Duncan Wyse explained that the Commerce Department is looking for and prioritizing "equity" in CHIPS Act applications that emphasize investments in places where semiconductor projects create job opportunities for the economically disadvantaged. At the January 30 meeting Keith Leavitt explained that "shared prosperity" underpins the Task Forces' work, and Representative Bynum noted that the Committee is committed to achieving "equity" in applying legislative land use decisions and actions and statewide application of the land use system.

Our January 30 Joint Committee testimony described our community's well-known and undisputed economically-disadvantaged status:

> "Cornelius is recognized by the State of Oregon as an economically Distressed Community due to low education levels, one of the lowest per capita incomes, and highest unemployment rate in Oregon. As of 2015, taxable assessed property values are roughly 48% of those for Washington County overall. Today, we have the highest population of Latinx residents in the state (after Woodburn) and one of the lowest per capita incomes in the Metro Region."

Joint Committee and Task Force consideration of two 500-acre semiconductor manufacturing fab sites near Cornelius presents an opportunity for the Legislature and Administration to deliver on their pursuit of "shared prosperity" and "workforce equity" by enabling semiconductor manufacturing supply chain companies to locate on our proposed 430-acre Cornelius UGB expansion site. Such home-based supply chain businesses will provide better-paying job opportunities - within our community - for many Cornelius households. This would help us address the burden on the 6,000 community members who must leave our community to work every day, with only 300 staying within the community for their employment.

V. Oregon Land Use System

Throughout the Joint Committee hearings there were many comments and suggestions about how to apply Oregon's Land Use (review and management) System to the Task Force's site recommendations. We understand the discussions to be centered on these main concerns: 1) the recommended 500-acre sites require moving prime farmland designated Rural Reserves into the Region's UGB (an oftentimes recipe for UGB expansion objections and delays); 2) the CHIPS Act 2-year funding decisions timeframe may not provide enough time to do that conclusively; 3) the System's long history of challenges to UGB expansion onto farmland creates both uncertainty in an administrative (LCDC) approval and probable resulting delay.

The need to demonstrate and assure timely land use "certainty" to the Commerce Department as well as to interested semiconductor manufacturing companies, who could be the private-sector partner with Oregon in a CHIPS Act application, was emphasized by Mr. Leavitt at the February 1 meeting. He noted that the more Oregon is able to complete UGB expansion, local site planning and regulations, permits, etc., the more "development certainty" becomes firm. In turn, this will attract private investment confidence for semiconductor manufacturing (as well as supply chain) companies. He also noted that the Commerce Department needs to see a site-development's "regulatory route" imminent (i.e., dependably affirmative) to be comfortable about Oregon's sites' state of "readiness."

Thus, such "certainty" would seem to require Legislative or Administrative approval of timely UGB expansions needed by Oregon semiconductor manufacturing and supply chain sites proposed for CHIPS Act funding. In short, a UGB expansion pathway referenced by Senator Knopp's February 8 remarks urging Legislators to "think big, be bold, not do things like they've always been done, be thoughtful but act with intent" because Committee failure (on the Land Use System issues) is not an option as so much (i.e., national security) is at stake.

Should the Committee or Administration decide to expand the UGB for both 500-acre sites for large new semiconductor chip manufacturing plants, it is justified and important to also expand the UGB next to Cornelius to support supply chain companies that do the "semiconductor assembly" work so essential to the production of those chips. Leaving the latter UGB expansion for supply chain companies out of a UGB expansion Bill would mean submitting an inadequate, incomplete Oregon CHIPS Act Application.

Finally, a UGB expansion into Rural Reserve land to enable chip manufacturing on the proposed 500-acre sites in Washington County presents an equally small leap – and large gains – for the Legislature or Administration to also approve the 430-acre UGB expansion onto Rural Reserve land next to Cornelius. Notably, at one time in the recent history of both sites their applicable land use policies contemplated future urban use of each site.

We truly hope your Committee finds these remarks helpful and supportive of recommending adding the 430-acre Cornelius site to Oregon's CHIPS Act Application as well as adding that land to any UGB expansion Bill under Committee consideration. We stand ready to help the Committee in whatever ways we can in large part because our proposed UGB expansion has long been and continues to be so very crucial to our City's current and future economic, social and environmental well-being.

Respectfully,

Jeffery Dalin, Mayor

John Colgan, City Council President

Angeles Godinez, City Councilor

Doris Gonzalez, City Councilor

Cc: U.S. Senator Ron Wyden
U.S. Senator Jeff Merkley
U.S. Representative Suzanne Bonamici
Vince Porter, Governor's Economic Policy Advisor
Oregon Semiconductor Competitiveness Task Force
Keith Leavitt, Port of Portland
Steve Callaway, Mayor, City of Hillsboro
Teri Lenahan, Mayor, City of North Plains

Attachments: 1. The Six-Step Semiconductor Chip Manufacturing Steps
2. Cornelius Urban Growth Boundary Request Area

Attachment 1: The Six-Step Semiconductor Chip Manufacturing Steps

Silicon: is a "semiconductor". It is a conduit of electrical currents; its conductive properties can increase when mixed with other materials such as phosphorus or born. Semiconductors, sometimes called integrated circuits (IC) or microchips, are made of pure elements, typically silicon or germanium or compounds. "Semiconductor" refers to a material whose conductivity.

A silicon chip is a very small piece of silicon that contains integrated circuits.

Chip: integrated circuit or small wafer of semiconductor material (i.e., silicon) embedded with integrated circuits. Chips comprise the processing unit and memory of the modern digital computer. Most microchips are made in China. 90% of most advanced chips made in Taiwan; 75% of production done in East Asia. *Taiwan Semiconductor Manufacturing Co*. (TSMC)

TSMC, Samsun & Intel: only firms capable of manufacturing advanced semiconductors.

Microchips ("chips"): Manufacturing chips: 6 semiconductor manufacturing steps: creating silicon wafer with working chips.

1. **deposition**: silicon wafer created; thin films for semiconducting materials deposited on waver to enable later printing on wafer. Wafer shrinking that involves using new materials and innovations enabling increased precision when depositing the coating.

2. **photoresist**; wafers covered w/ light-sensitive coating ("photoresist" or "resist"). Positive resist (used in most semiconductor manufacturing) has higher resolutions which is better for lithography stage work. "Resist" is produced for semiconductor manufacturing by suppliers (Dow Chemical, Fuji Films, etc.)

3. **lithography**: Crucial chip-making step: done by lithography machine (Intel wanted CHIPS $$ for on-site lithography-works facility). Process determines how small a chip can be. Chip wafer exposed to ultraviolet light used to produce finest (smallest) details of the chip.

4. **etching:** removes degraded "resist" to show intended pattern. Chip wafer is baked and developed to reveal a 3D pattern of open channels. Etch processes imprints conductive features of the wafer. Etch companies to this work (another supplier) (Lam Research, Oxford Instruments, SEMES) Chips will have multiple microchip layers structure.

5. **ionization: Ion implant:** After etching, wafer is bombarded with positive and negative ions that refine the electrical conducting properties of its patterns. Applying charged ions into silicon crystal allows the flow of electricity to be controlled and transistors _ electronic switches that are basic building blocks of microchips – to be created.

6. **packaging:** To get the chips out of the wafer, the wafer is then sliced and diced into individual chips (most common size is 300-mm wafer most often used in semiconductor manufacturing) creating "chip dies". Dies then placed onto a "substrate" – a baseboard that uses metal foils to direct chip input and output signals to other parts of a system. (Also done by suppliers like Applied Materials, Ayar Labs, SPTS Technologies, Wiliot Ayers)

Attachment 2: Cornelius Urban Growth Boundary Request Area Map